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Analysis and Simulation of a Symmetric Multilevel Inverter Topology

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ABSTRACT: In this study, a symmetrical source-based multilevel inverter capable of generating an 11-level output voltage is introduced. The main objective of the proposed topology is to minimize the number of inverter components while enhancing voltage step generation. The developed configuration produces an 11-level staircase output waveform that closely resembles a sinusoidal waveform without increasing the count of power semiconductor switches. To regulate the inverter operation, a Carrier-Based Sinusoidal Pulse Width Modulation (CB-PWM) technique is employed at a switching frequency of 3 kHz. The simulation analysis is performed using the MATLAB/Simulink R2019b platform. The operating principle of the proposed MLI is thoroughly described. This work emphasizes the design of a novel single-phase multilevel inverter with a reduced component requirement. The proposed configuration is arranged to achieve the highest possible number of voltage levels in the AC output while using fewer power electronic devices. Additionally, the inverter performance is evaluated at a modulation index of 1 under RL load conditions to study its dynamic response and voltage level generation capability.

I. INTRODUCTION

Multilevel inverters (MLIs) have emerged as a key technology in modern power electronic converters due to their extensive industrial applications and technical advantages [1]–[3]. With the rapid growth in electrical energy demand, the integration of MLIs into advanced power conversion systems has become increasingly important [4], [5]. These converters are widely employed in variable-speed drives, electric vehicles, and high-voltage DC (HVDC) transmission systems [6]–[8]. Furthermore, MLIs play a significant role in renewable energy conversion systems such as photovoltaic and wind energy applications [9], [10]. They are particularly suitable for medium-voltage and high-power operations [11]. In multilevel inverters, higher voltage levels are synthesized by combining multiple DC sources to produce a stepped output waveform [12]. This staircase waveform closely approximates a sinusoidal signal, resulting in lower total harmonic distortion (THD) [13], [14]. Consequently, the requirement for bulky output filters is reduced. Additionally, the stepped voltage transition decreases dv/dt stress across the switching devices [15]. Since each switch experiences reduced voltage stress, lower-rated semiconductor devices can be used, making the system more economical [16]. Many MLI topologies also provide redundant switching states that can be utilized for fault-tolerant operation [17]. The three conventional multilevel inverter structures developed historically are the Neutral Point Clamped (NPC), Flying Capacitor (FC), and Cascaded H-Bridge (CHB) topologies [18]–[20]. Although these classical configurations offer several advantages over traditional two-level inverters, they suffer from drawbacks such as a large number of power switches, multiple DC sources, and numerous capacitors [21]. To address these limitations, several modified and reduced-component MLI topologies have been proposed to improve efficiency and minimize hardware requirements [22]. These modern configurations are generally classified into symmetrical and asymmetrical types based on the magnitude of the DC voltage sources. Various modulation techniques such as Selective Harmonic Elimination (SHE), Space Vector PWM (SVPWM), Carrier-Based PWM (CB-PWM), and Nearest Level Control (NLC) have also been developed to enhance MLI performance [13], [22].

This paper introduces a symmetrical 11-level multilevel inverter (MLI) topology. The effectiveness of the proposed configuration is analyzed through MATLAB/Simulink simulations under RL load conditions at various modulation indices. The organization of the paper is structured as follows: Section 3 explains the operational principles and the modulation strategy adopted for the proposed inverter; Section 4 details the different operating states; and Section 5 outlines the simulation setup along with the corresponding results and discussion.

II. PROPOSED TOPOLOGY

The configuration of the proposed 13-level MLI is illustrated in Fig. 1. The overall structure is divided into two main functional sections: the level generation unit and the polarity generation unit. The topology employs a total of thirteen power semiconductor switches. These switches are classified according to their operating characteristics. Switches S_5 , S_8 , S_9 , S_{12} and S_{13} function as bidirectional switches, enabling current to flow in both directions. This feature is essential for flexible voltage level formation and ensures proper operation in all four quadrants. The remaining switches, operate as conventional unidirectional switches. The inverter operates in a symmetrical configuration, where all six DC voltage sources have identical magnitudes. This symmetrical arrangement provides important benefits, such as uniform voltage stress distribution across the switches and simplified control and modulation implementation. The level generation unit is responsible for producing the stepped DC voltage levels. By appropriately turning on selected switches, the circuit either connects or bypasses the five equal DC sources in different series combinations to obtain the required intermediate voltage levels. The polarity generation unit consists of four switches configured as a full-bridge inverter. This unit converts the generated stepped DC voltage into both positive and negative half-

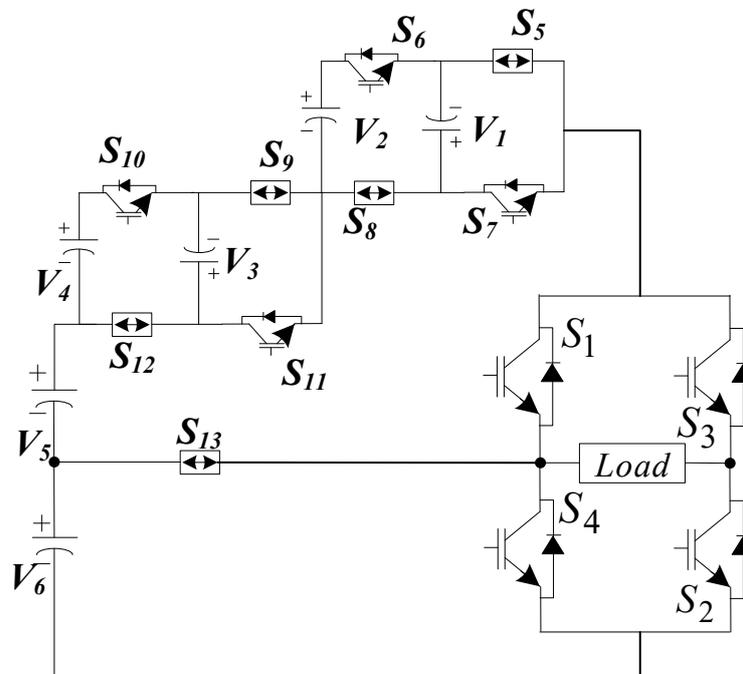
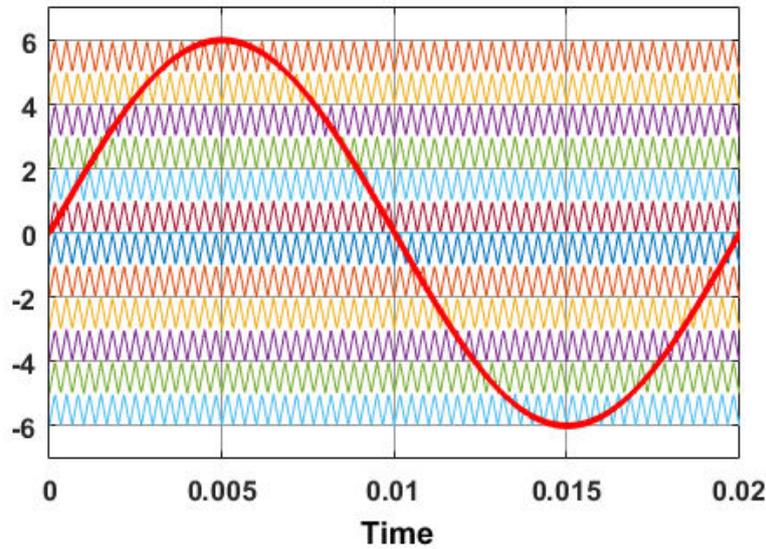


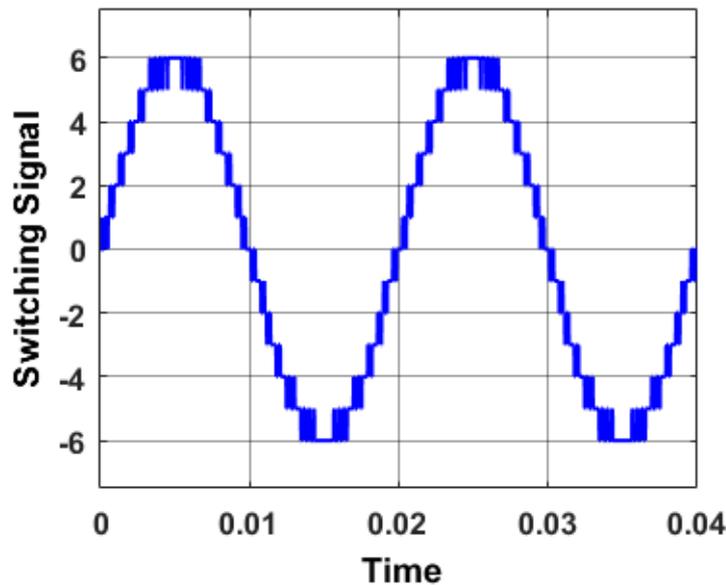
Fig. 1. Proposed MLI topology

III. MODULATION AND CONTROL OF MLI

In the 13-level multilevel inverter illustrated in Fig. 2(a), a low-frequency sinusoidal reference signal is compared with several high-frequency triangular carrier signals. For a 13-level output, twelve carrier waves are used, each operating at approximately 3 kHz. The sinusoidal reference determines the fundamental frequency of the output waveform, while its amplitude defines the modulation index and consequently regulates the output voltage magnitude. Switching pulses are generated whenever the reference sine wave intersects with any of the carrier signals. As the reference signal progresses through different carrier regions, the inverter transitions among multiple discrete voltage levels, resulting in thirteen output levels—six positive levels, six negative levels, and one zero level. This switching process produces a staircase-shaped output waveform that closely resembles a sinusoidal waveform. As a result, total harmonic distortion (THD) is significantly reduced, dv/dt stress across the switching devices is minimized, and the overall quality of the output voltage is enhanced. Fig. 2(b) presents the stepped output voltage waveform obtained from this modulation scheme.



(a)



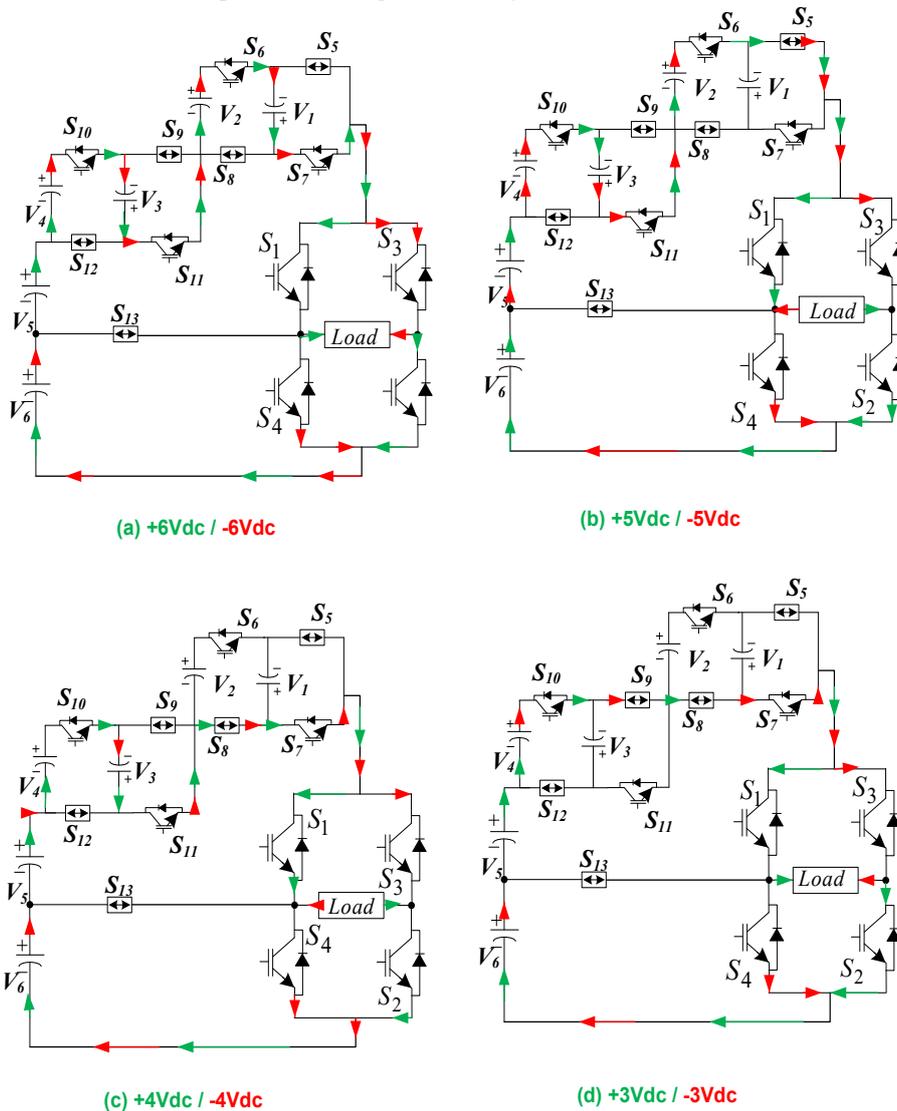
(b)

Fig. 2: Pulse-width modulation process: (a) Reference sine wave compared with carrier signals; (b) Generated switching waveform for the 13-level inverter.

IV. MODES OF OPERATION

The proposed inverter generates its thirteen distinct output voltage levels by implementing specific switching configurations, which are detailed in Table 1. In this scheme, a check mark (✓) indicates that a switch is turned ON, while a cross (×) means it remains OFF. To generate the positive half-cycle, the +6Vdc level is produced by activating switches S1, S2, S6, S7, S10, and S11. The +5Vdc level is achieved by turning on S1, S2, S5, S6, S10, and S11. For +4Vdc, switches S1, S2, S7, S8, S10, and S11 are used. The +3Vdc level is created by conducting S1, S2, S7, S8, S9, and S10, while +2Vdc requires S1, S2, S7, S8, S11, and S12. The lowest positive level, +1Vdc, is obtained by activating S2, S7, S8, and S13. The zero-voltage state (0Vdc) is achieved with only S2 and S4 turned on.

The negative voltage levels are produced by reversing the current path within the polarity generation unit. The $-1V_{dc}$ level is created when switches S_7 , S_8 , S_{11} , S_{12} , and S_{13} are on. For $-2V_{dc}$, the conducting switches are S_3 , S_4 , S_7 , S_8 , S_{11} , and S_{12} . The $-3V_{dc}$ level is generated by S_3 , S_7 , S_8 , S_9 , and S_{10} . To achieve $-4V_{dc}$, switches S_3 , S_4 , S_7 , S_8 , S_{10} , and S_{11} are activated. The $-5V_{dc}$ level is formed by turning on S_3 , S_4 , S_5 , S_6 , S_{10} , and S_{11} . Finally, the most negative level, $-6V_{dc}$, is produced by conducting S_3 , S_4 , S_6 , S_7 , S_{10} , and S_{11} . In summary, each of the thirteen voltage levels corresponds to a unique switching state. These states strategically connect or bypass the DC sources to synthesize the desired stepped AC output waveform. The switching modes for generating these voltage levels are illustrated in Fig. 4. In these diagrams, the green arrow represents the current path during the positive half-cycle, while the red arrow indicates the conduction path for the negative half-cycle.



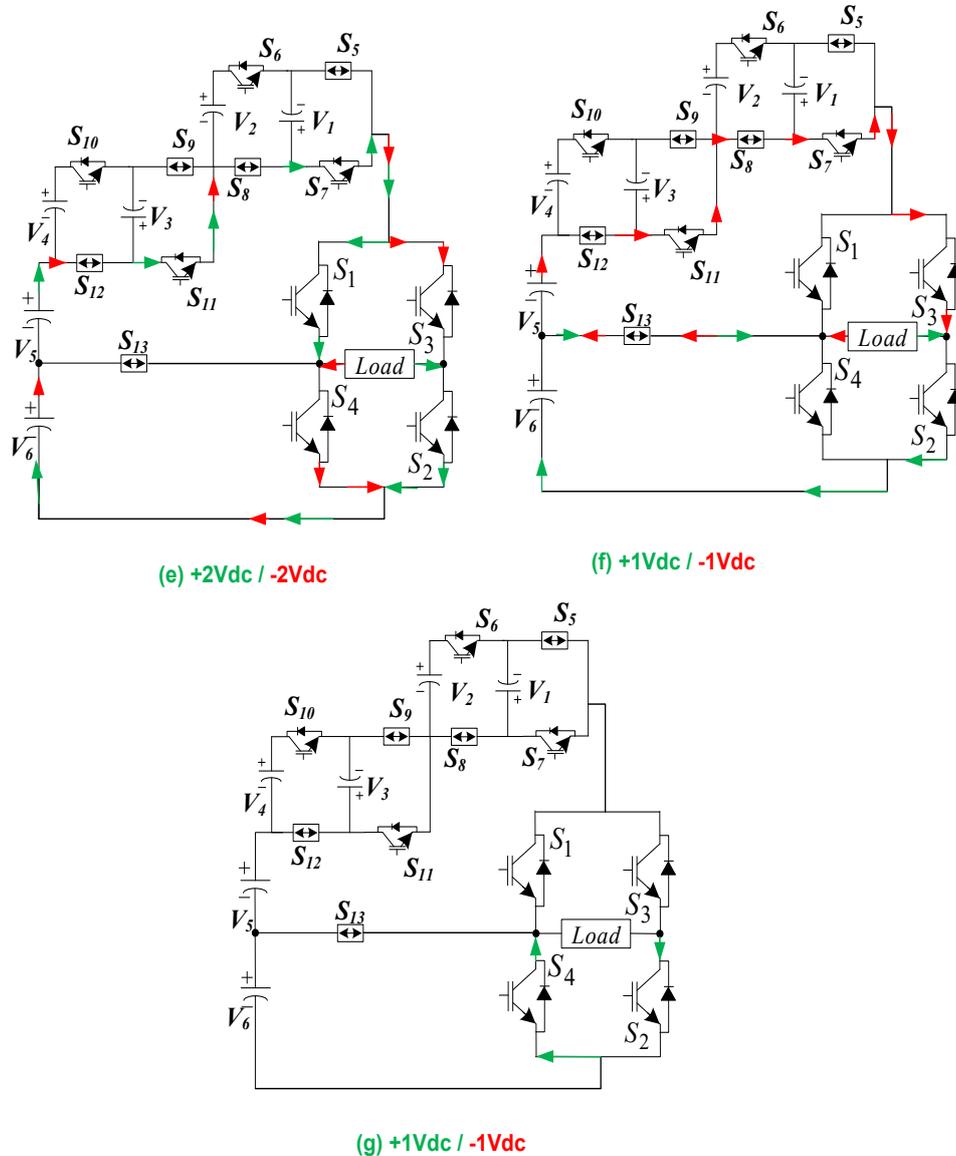


Fig.4. Modes of operation for positive and negative half cycle of the proposed MLI

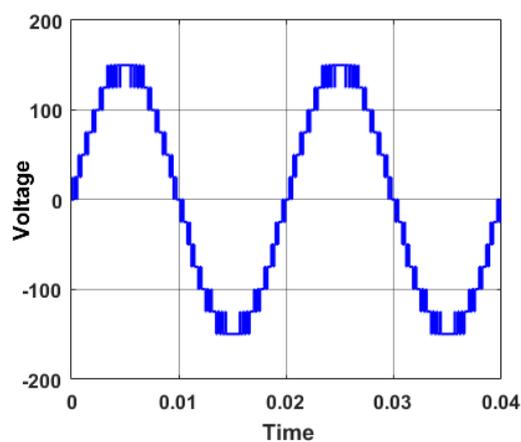
Table. 1. Switching status of proposed MLI

	S ₁	S ₂	S ₃	S ₄	S ₅	S ₆	S ₇	S ₈	S ₉	S ₁₀	S ₁₁
+6V _{dc}	✓	✓	✗	✗	✗	✓	✓	✗	✗	✗	✗
+5V _{dc}	✓	✓	✗	✗	✓	✓	✗	✗	✗	✗	✗
+4V _{dc}	✓	✓	✗	✗	✗	✗	✓	✓	✗	✗	✗
+3V _{dc}	✗	✓	✗	✗	✗	✗	✗	✗	✓	✗	✗

+2V _{dc}	X	✓	X	X	X	X	X	X	X	✓	X
+1V _{dc}	X	✓	X	X	X	X	X	X	X	X	✓
0V _{dc}	X	✓	X	✓	X	X	X	X	X	X	X
-1V _{dc}	X	X	✓	X	X	X	✓	✓	✓	X	X
-2V _{dc}	X	X	✓	X	X	X	✓	✓	✓	X	X
-3V _{dc}	X	X	✓	X	X	X	✓	✓	X	✓	X
-4V _{dc}	X	X	✓	✓	X	X	✓	✓	X	X	X
-5V _{dc}	X	X	✓	✓	✓	✓	X	X	X	X	X
-6V _{dc}	X	X	✓	✓		✓	✓	X	X	X	X

V. SIMULATION AND EXPERIMENTAL RESULTS

This section presents the simulation results validating the performance of the proposed 13-level inverter topology. A detailed model was developed using the MATLAB/Simulink R2019b environment. The inverter employs a symmetrical configuration of six DC sources (V1 through V6), each rated at 40 V. This arrangement of equal voltages enables the generation of 13 distinct output voltage steps. The system was tested at a modulation index of 1, driving an RL load consisting of a 50 Ω resistor in series with a 75 mH inductor. The simulation results confirm a maximum output voltage of 240 V and a peak load current of 1.6 A.



(a)

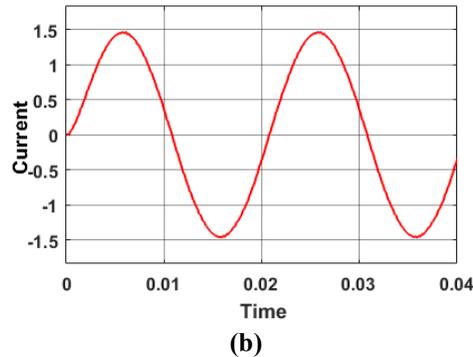


Fig. 4. Simulation results for the (a) output voltage; (b) load current; at MI = 1

VI. CONCLUSION

This paper presents a symmetrical 13-level MLI topology designed with a reduced component count, utilizing only eleven switches. The architecture is strategically divided into a level generation unit and a polarity generation unit incorporating four bidirectional switches to manage current flow. By employing a symmetrical arrangement of six 25 V DC sources, the design ensures balanced voltage stress across components and simplifies the modulation strategy. Through the selective series connection of these sources, the inverter reliably synthesizes thirteen distinct voltage levels, including zero, thereby enhancing the harmonic profile of the output waveform. The feasibility of the proposed topology was validated through simulations conducted in MATLAB/Simulink R2019b. Under an RL load with $R=100\ \Omega$, and $L=80\ \text{mH}$ and a modulation index of 1, the inverter successfully produced a maximum output voltage of 150 V and a peak load current of 1.6 A, confirming its operational integrity. In conclusion, the proposed inverter achieves a compact and efficient design, balancing a reduced switch count with high-quality voltage generation, which positions it as a viable candidate for medium-voltage and renewable energy applications.

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